In the Claims:

**Claim 1 (Currently Amended)**

A control system, comprising:

a storage device to store data signals and a mode designator, the mode designator to select a first or a second mode of operation;

a circuit coupled to the storage device to receive as control signals predetermined ones of the data signals along with the mode designator, the control signals to control operation of the circuit when the circuit is operating in [a] the first mode; and

Error Correction Code (ECC) logic coupled to the storage device to interpret the predetermined ones of the data signals as ECC check bits to detect errors in the data signals when the circuit is operating in [a] the second mode.

**Claim 2 (Original)**

The system of Claim 1, wherein the storage device is a memory having multiple addressable storage locations, each storing a different respective set of data signals.

**Claim 3 (Original)**

The system of Claim 2, wherein each of the addressable storage locations includes circuits to store a respective mode designator to control whether the circuit operates in the first or the second mode after the data signals stored at the addressable storage location are read from the memory.

**Claim 4 (Original)**

The system of Claim 3, wherein the circuit includes branch logic to utilize the predetermined ones of the data signals stored at an addressable storage location to generate a next address for addressing the memory if the mode designator stored at the addressable storage location indicates the circuit will operate in the first mode.

**Claim 5 (Canceled)**

**Claim 6 (Original)**

The system of Claim 1, wherein the circuit includes logic to provide one or more functions of an instruction processor.

**Claim 7 (Original)**

The system of Claim 1, and further including a programmable storage device coupled to the circuit to select the predetermined ones of the data signals.

**Claim 8 (Original)**

The system of Claim 1, and further including at least one parity circuit coupled to the storage device to determine whether a parity error occurred on any of a predetermined set of the data signals.

**Claim 9 (Original)**

The system of Claim 8, wherein the at least one parity circuit includes a circuit to determine whether a parity error occurred on the predetermined set of the data signals when the circuit is operating in the second mode.

**Claim 10 (Original)**

The system of Claim 1, wherein the ECC logic is coupled to ECC complement logic to correct errors in the data signals that are detected by the ECC logic when operating in the second mode.

**Claim 11 (Original)**

The system of Claim 10, and further including logic coupled to the ECC complement logic to provide the data signals to the circuit for use as control signals after any errors detected by the ECC logic have been corrected.

**Claim 12 (Currently Amended)**

A method of controlling a digital system, comprising:

a.) reading first data signals along with a mode indicator from a storage device;

b.) interpreting the first data signals as control signals to control one or more functions of the digital system if operating in a first mode of operation as determined by a state of the mode indicator; and

c.) interpreting the first data signals as Error Correction Code (ECC) signals if operating in a second mode of operation as determined by the state of the mode indicator.

**Claim 13 (Original)**

The method of Claim 12, and further including:

reading second data signals from the storage device; and

using the ECC signals to detect errors in the second data signals if operating in the second mode of operation.

**Claim 14 (Original)**

The method of Claim 13, wherein the storage device is a memory, and wherein the first and second data signals are stored at a same addressable location within the memory.

**Claim 15 (Original)**

The method of Claim 14, wherein multiple memory addresses each stores different respective first and second data signals.

**Claim 16 (Original)**

The method of Claim 15, and further including using the first data signals to generate a next address for addressing the memory when operating in the first mode of operation.

**Claim 17 (Currently Amended)**

The method of Claim 15, and further including:

reading one of the multiple memory addresses; and

interpreting at least one of the second data signals as [a] the mode indicator to indicate whether operation is occurring in the first or the second mode of operation.

**Claim 18 (Currently Amended)**

The method of Claim 17, and including repeating the steps of Claim 17 for each of multiple memory addresses.

**Claim 19 (Original)**

The method of Claim 13, and further including, correcting an error if the error is detected in predetermined ones of the second data signals.

**Claim 20 (Original)**

The method of Claim 19, and further including programmably selecting the predetermined ones of the second data signals.

**Claim 21 (Original)**

The method of Claim 12, and further including programmably selecting the first data signals.

**Claim 22 (Original)**

The method of Claim 13, and further including interpreting one or more of the second data signals as control signals to control an arithmetic logic unit of an instruction processor.

**Claim 23 (Original)**

The method of Claim 13, an further including using parity bits to detect a parity error occurring within the first or the second data signals.

**Claim 24 (Original)**

The method of Claim 23, and further including:

reporting any error detected using the ECC signals; and

reporting any error detected using the parity bits.

**Claim 25 (Original)**

The method of Claim 24, and further including:

servicing any error detected by the ECC signals at a time that is optimal for the digital system; and

servicing any error detected using the parity bits substantially immediately.

**Claim 26 (Currently Amended)**

A control system having a first and second mode of operation, comprising:

storage means for storing data signals and a mode designator, a state of the mode designator selecting between operation in the first mode or the second mode;

control means for receiving the data signals with the mode designator, and for utilizing first ones of the data signals to affect operations of the control system when operating in the first mode; and

error means for interpreting the first ones of the data signals as check bits for detecting errors occurring in second ones of the data signals when the control system is operating in the second mode.

**Claim 27 (Currently Amended)**

The system of Claim 26, wherein the storage means includes means for storing [a] the mode designator to control whether the control system is operating in the first or the second mode.

**Claim 28 (Original)**

The system of Claim 26, wherein the control means includes branch means for utilizing the first ones of the data signals to generate an address for the storage means.

**Claim 29 (Original)**

The system of Claim 26, wherein the storage means is a memory including predetermined addressable locations, each storing a different respective set of the first and second ones of the data signals.

**Claim 30 (Original)**

The system of Claim 29, wherein each of the predetermined addressable locations within the memory includes means for storing a mode designator for controlling whether the control system operates in the first or the second mode when the first and the second ones of the data signals stored at the addressable location are read from the memory.

**Claim 31 (Original)**

The system of Claim 30, wherein the error means includes means for correcting an error detected on predetermined ones of the second ones of the data signals when the control system is operating in the second mode.

**Claim 32 (Original)**

The system of Claim 31, and further including means for providing corrected ones of the second ones of the data signals to the control means for use in affecting the operations of the control system.

**Claim 33 (Original)**

The system of Claim 31, and further including parity detection means for detecting parity errors within the first or the second ones of the data signals.

**Claim 34 (Original)**

The system of Claim 33, wherein the parity detection means includes means for detecting uncorrected parity errors remaining within the second ones of the data signals.

**Claim 35 (Original)**

The system of Claim 33, and further including maintenance means for performing error recovery actions within a first time period for errors detected by the parity detection means and, for errors detected by the error means, performing error recovery actions any time the control system is appropriately configured.

**Claim 36 (Original)**

The system of Claim 26, and further including means for programmably selecting the first ones of the data signals.

**Claim 37 (Original)**

The system of Claim 31, and further including means for programmably selecting the predetermined ones of the second ones of the data signals.